AMENDMENTS TO THE CLAIMS:

Please cancel claims 1, 5-17 without prejudice. Claims 18-20 have been added.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (cancelled)

Claim 2 (original): A semiconductor integrated circuit having an AND logic circuit which comprises:

a NAND circuit which includes:

parallel-connected first and second p-channel MOS FETs, where first and second input signals are respectively input into the gate electrodes of the FETs; and

a first n-channel MOS FET, where the first input signal is input into the gate electrode and an inverted signal of the second input signal is input into the source electrode, and

wherein the common drain electrode of the first and second p-channel MOS FETs and the drain electrode of the first n-channel MOS FET are connected; and

an inverter circuit having a complementary MOS transistor structure for receiving an output signal from the NAND circuit and outputting an inverted signal of the received signal from an output terminal, where the complementary MOS transistor structure comprises a third p-channel MOS FET and a second n-channel MOS FET, and

wherein among all the MOS FETs in the AND logic circuit, each FET other than the third p-channel MOS FET has a threshold voltage value lower than the threshold voltage value of the third p-channel MOS FET.

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Claim 3 (original): A semiconductor integrated circuit having an AND logic circuit which comprises:

a NAND circuit which includes:

a first pMOS FET, where a fixed electric potential is applied to the gate electrode so as to keep the first MOS FET on; and

a first n-channel MOS FET, where a first input signal is input into the gate electrode and a second inverted input signal is input into the source electrode; and

wherein the drain electrode of the first p-channel MOS FET and the drain electrode of the first n-channel MOS FET are connected; and

an inverter circuit having a complementary MOS transistor structure for receiving an output signal from the NAND circuit and outputting an inverted signal of the received signal from an output terminal, where the complementary MOS transistor structure comprises a second p-channel MOS FET and a second n-channel MOS FET, and

wherein among all the MOS FETs in the AND logic circuit, each FET other than the second p-channel MOS FET has a threshold voltage value lower than the threshold voltage value of the second p-channel MOS FET.

Claim 4 (original): A semiconductor integrated circuit having a NOR logic circuit which comprises:

a first pMOS FET, where a first input signal is input into the gate electrode and an inverted signal of a second input signal is input into the source electrode; and

parallel-connected first and second nMOS FETs, where the first and second input signals are respectively input into the gate electrodes of the FETs, and wherein:

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the drain electrode of first pMOS FET and the common drain electrode of the first and second nMOS FETs are connected; and

the threshold voltage value of each of the MOS FETs is the NOR logic circuit may be decreased.

Claim 5 - 17 (cancelled)

Claim 18 (new): A semiconductor integrated circuit as claimed in claim 2, wherein the logic circuit is applied to a decoder circuit.

Claim 19 (new): A semiconductor integrated circuit as claimed in claim 3, wherein the logic circuit is applied to a decoder circuit.

Claim 20 (new): A semiconductor integrated circuit as claimed in claim 4, wherein the logic circuit is applied to a decoder circuit.

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